CHAPTER 10: The CPU

PASTPAPERS

N.B. These pastpapers may rely on the knowledge gained from the **previous chapters.**

1 SEC’94-PAPER 1-Q3B

Briefly explain the purpose of the PROGRAM COUNTER **[2]**

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2 SEC'94-PAPER 2A-Q4

(a) Why is a 16-bit 60 MHz CPU generally faster than an 8-bit 12 MHz CPU? **[4]**

(b) Describe how the CPU can read from and write to main memory using the **address bus** and the **data bus**. **[4]**

(c) Briefly describe the **fetch-execute** cycle **[6]**

(d) What is meant by a CPU's **instruction set**? **[2]**

Writing Space for Previous Question

3 SEC'95-PAPER 2A-Q4A (CONSULT CH 5)

a. A 16-bit computer uses a 20-bit address register.

i. What is the size of the addressable memory for this computer? **[1]**

ii. What is the word length for this computer? **[1]**

iii. How many memory cycles does the CPU need to fetch a four-byte instruction using this computer? **[2]**

4 SEC'97-PAPER 2B-Q3D

How does the number of bits in the Memory Address Register affect the amount of memory that can be addressed by the computer? **[2]**

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5 SEC'97-PAPER 2B-Q7B

Three **registers** normally found in a computer are:

- *Memory Address Register*
- *Accumulator*
- *Program Counter*

For each of these registers include:

i. the Unit in which it is found; **[3]**

ii. and its purpose. **[6]**

6 SEC'98-PAPER 2A-Q4A

a. Explain the function of the following parts of the CPU:

i. control unit **[1]**

ii. program counter **[1]**

iii. instruction register **[1]**

Hence briefly describe the fetch-execute cycle of the CPU. **[3]**

7 SEC'98-PAPER 2B-Q4B

b. Mention **TWO** registers normally found in the CPU, and explain the function of each. **[6]**

8 SEC'99-PAPER 2B-Q6C

Communications inside a computer are carried out over the system bus, which includes the ***data bus*** and the ***address bus***.

(a) What is the difference between the ***data bus*** and the ***address bus***? **[4]**

(b) How does the number of lines in the data bus affect the ***performance*** of a computer? **[2]**

(c) How does the number of lines in the address bus determine the ***address space*** of the CPU? **[2]**

9 SEC '00-PAPER 1-Q1 (CONSULT CH 7)

What is each of the following called?

A CPU register in which the address of the instruction being executed is held:_____ **[1]**

Data on which an instruction is to operate: _____ **[1]**

The amount of memory a CPU can access: _____ **[1]**

The bus over which instructions are transferred from main memory to the CPU: _____ **[1]**

10 SEC '01-PAPER 1-Q10

The following are the main steps of the Fetch Execute cycle performed repeatedly by the Central Processing Unit. The steps have been jumbled up. Indicate the correct sequence of the cycle by writing the corresponding letter from the table in the spaces provided below.

a	Activate correct circuits for instruction to be obeyed.
b	Increment value in program counter by 1.
c	Repeat second step.
d	Fetch the instruction from the memory location specified by the program counter.
e	Move any results from the accumulator back to the main memory.
f	Set the value of the program counter to the address of the first instruction.
g	Decode the instruction and fetch any data required by the instruction from central memory and place it in storage locations within the accumulator of the arithmetic and logic unit.

Step 1 letter _____ Step 2 letter _____ Step 3 letter _____
Step 4 letter _____ Step 5 letter _____ Step 6 letter _____
Step 7 letter _____ **[3]**

11 SEC '01-PAPER 2B-Q4 (CONCULT CH 2 & 7)

(a) What do the letters **CPU** stand for? **[1]**

(b) Draw a block diagram which illustrates the FOUR main units of computer hardware system. In your answer show the directions of data flow between the components. **[2]**

(c) Write short descriptions of each of the following pairs of hardware terms

i. ***CPU*** and ***ALU*** **[2]**
ii. ***Internal*** and ***external (main) memory*** **[2]**
iii. ***Accumulator*** and ***program counter*** **[2]**
iv. ***Address*** and ***data bus*** **[2]**

(d) When a program is loaded into memory and run, the *fetch execute cycle comes* into play. Explain the steps involved. **[4]**

(e) The computer's **wordlength** has a significant effect on the overall performance of a computer system. Explain. **[2]**

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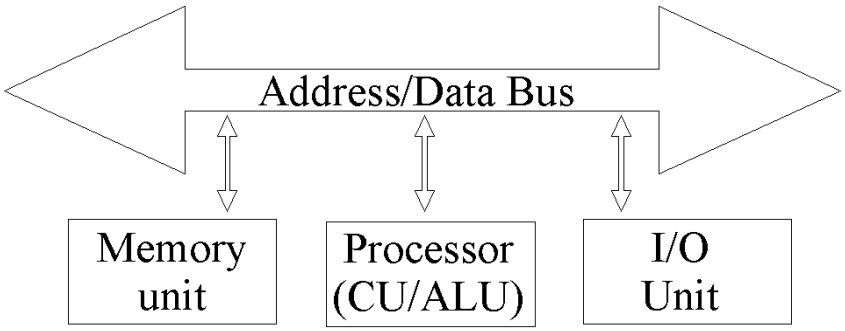
Writing Space for Previous Question

12 SEC '02-PAPER 2A-Q7 (CONSULT CH 5 & 7)

As shown in the figure below, a computer consists of functional units connected together by means of a bus system.
(CU: Control Unit)
(ALU: Arithmetic and Logic Unit)



(a) Briefly describe the function of the control unit, arithmetic and logic unit, and memory unit. **[3]**

(b) Distinguish between address bus and data bus. **[2]**

(c) Write down the steps involved in running a program that has been previously loaded into the memory unit. **[3]**

(d) If a given instruction uses up 6 clock cycles, how much time, in nanoseconds, does it take to execute it using a 1.5Ghz processor? **[3]**

(e) What is the maximum amount of memory, in gigabytes, that may be directly addressed by a 32-bit address bus? **[3]**

(f) Explain what is meant by the term 'RAM'. Give a typical use of RAM. **[3]**

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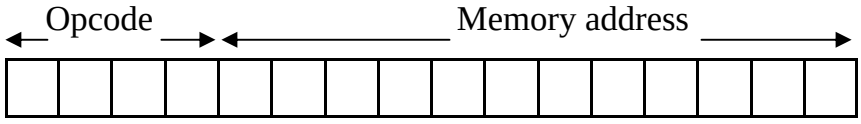
Writing Space for Previous Question

13 SEC '03-PAPER 1 Q11 (CONSULT CH 5)

A single machine-code instruction of a 4-bit function code (opcode) and a 12-bit memory address.



a. What is the maximum number of possible function codes (opcodes)? **[2]**

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b. What is the number of locations which can be directly addressed?

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c. The **accumulator** and the **program counter** are two registers found in the CPU. For each register, state its use and identify the part of the CPU in which it is found.

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14 SEC '04-PAPER 2A Q4

(a) What is the purpose of the following CPU registers: Program Counter (PC), Current Instruction Register (CIR) **[2]**

(b) Refer to the registers mentioned in (a) to briefly describe the *fetch-execute* cycle used to run a program stored in the main computer memory. **[5]**

15 SEC '04-PAPER 2B Q6 (CONSULT CHs 2,4,5,7 & 8)

(a) For each of the following statements state whether it is true or false:
(i) the fetch-execute cycle's role is to write information to the hard-disk;
(ii) primary memory is faster than secondary storage;
(iii) OCR devices read text. **[3]**

(b) Mention **TWO** properties of each of the following hardware components:
(i) CPU; (iii) ROM;
(ii) RAM; (iv) Buses. **[8]**

(c) A particular system uses 9 bits to store a character. The *leftmost* bit is used for *odd partiy* and the *rest* holds the *character code.*
The word '**CAB**' is to be written in memory starting at address 128000. The character code in binary for A is 01000001 (65 in decimal). The code for B is obtained by adding 1 to the code of A (i.e. ASCII code of character B in decimal is 66), whereas that of C is similarly obtained by adding 1 to the code of B (i.e. ASCII code of character C in decimal is 67).
Copy and complete the diagram below to show the contents (in binary) of the three locations starting at 128000. (The memory location storing letter 'A' of word 'CAB' is given.)

Address	Parity bit, Character code	Character
128000		'C'
128001	1 01000001	'A'
128002		'B'

[6]

Writing Space for Previous Question

16 SEC '05-PAPER 1 Q7 (CONSULT CHs 4 & 8)

Mention an appropriate unit of measurement associated with each of the following hardware device types. The first one is given.

(i) LAN cable: *megabits per second*

(ii) CPU: …… **[1]**

(iii) Printer: ……. **[1]**

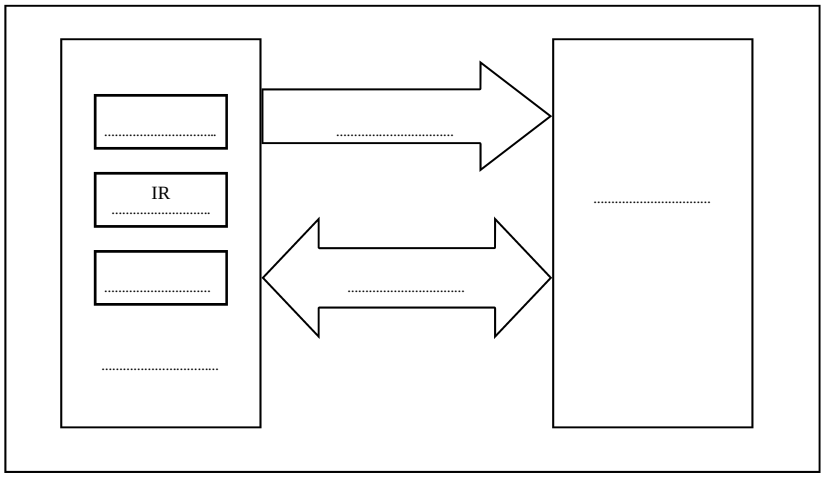
(iv) Scanner: …….. **[1]**

(v) Hard disk access time: ……. **[1]**

(vi) Modem: ……. **[1]**

17 SEC '05-PAPER 1 Q10

(a) Use the given words to label the block diagram below. The first one is given. **[3]**



instruction register (IR) *address bus (ADBUS)* *memory (MEM)*
program counter (PC) *accumulator (ACCM)* *data bus (DTBUS)*
central processing unit (CPU)

(b) Referring to the above diagram, briefly describe the fetch-execute cycle. **[4]**

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18 SEC '05-PAPER 2A Q8 (CONSULT CHs 2 & 8)

(a) Digital computers use *binary values* to store and process data.

(i) What are the TWO possible values that a single binary digit can have? **[1]**

(ii) What is a *byte* and what is a *word?* **[2]**

(iii) What function does the *parity bit* serve? WHEN and HOW is the parity bit used? **[4]**

(iv) Explain, very briefly, why the single parity system cannot detect all possible errors. **[2]**

(b) Describe, very briefly, the main differences between *serial transmission* and *parallel transmission* of data. **[2]**

(c) The CPU contains registers.

(i) What is a register and what is it used for? **[2]**

(ii) What is an accumulator used for? **[2]**

(d) During the fetch-execute cycle:

(i) What determines the memory location from which the next institution is fetched? **[1]**

(ii) Give an example of an instruction which changes the location from which the next instruction is fetched. **[1]**

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Writing Space for Previous Question

19 SEC '06-PAPER 1 Q2 (CONSULT CH 8)

State whether each of these is **True** or **False**

(a) Video-conferencing is a synchronous form of communication. _____ **[1]**

(b) Online shopping requires network access. _____ **[1]**

(c) Access to online help requires network access facilities. _____ **[1]**

(d) Electronic mail is an asynchronous form of communication. _____ **[1]**

(e) Another term for the Internet is WWW (World Wide Web). _____ **[1]**

20 SEC '06-PAPER 2A Q7 (CONSULT CHs 5 & 6)

A logic circuit has two inputs A1 and A2 and two outputs P and Q. Output P is 1 when either one of the inputs is 1 but not both. Output Q is 1 when the two inputs are 1.

a) Complete the truth table for this circuit **[2]**

A1	A2	P	Q
0	0		
0	1		
1	0		
1	1		

b) Using AND, OR and NOT gates, draw the logic circuit for outputting P and Q given inputs A1 and A2. **[4]**

c) Write down the two Boolean expressions for obtaining outputs P and Q. **[4]**

d) Given that A1 and A2 are binary digits, name the arithmetic operation implemented by the logic circuit and hence identify the outputs P and Q. **[2]**

e) Give TWO uses for the computer's Data Bus. **[2]**

f) An 8-bit register is used to store signed integers in two's complement notation. Write down the binary pattern for storing –39 in this register. **[3]**

Writing Space for Previous Question

21 SEC '07-PAPER 1 Q11 (CONSULT CHs 5 & 7)

A given computer has a 20-bit address bus.

a) (i) What amount of memory locations are directly addressable? **[2]**

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(ii) Identify another bus structure of the computer and state its use. **[2]**

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b) The **Instruction Register** and the **Program Counter** are two registers found in the CPU. State the use of each register. **[2]**

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